

AUG 01 2005

PTO/BB/21 (09-04)

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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Patent Number	6,185,707 B1
	Issue Date	February 6, 2001
	First Named Inventor	Shawn Smith
	Art Unit	N/A
	Examiner Name	Albert De Cady
Total Number of Pages in This Submission	Attorney Docket Number	014823-116

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input checked="" type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Statement under 37 CFR 3.73(b) (7 pages)
Remarks <div style="font-size: 2em; text-align: center;">25784</div>		

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Printed name	Michael O. Scheinberg		
Date	August 1, 2005	Reg. No.	36,919

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Patent Number	6,185,707
Issue Date	February 6, 2001
First Named Inventor	Shawn Smith
Art Unit	N/A
Examiner Name	Albert De Cady
Attorney Docket Number	014823-116

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners associated with the Customer Number:

25,784

☒ Please change the correspondence address for the above-identified application to:☒ The address associated with  
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OR

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Address	P.O. Box 164140				
City	Austin	State	TX	Zip	78716-4140
Country	USA				
Telephone	(503) 726-7500	Fax	(512) 306-1963		

I am the:

☐ Applicant/Inventor.☒ Assignee of record of the entire interest. See 37 CFR 3.71.  
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

## SIGNATURE of Applicant or Assignee of Record

Signature 

Name Bradley J. Thies

Date 8/1/05 Telephone (503) 726-7500

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

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**STATEMENT UNDER 37 CFR 3.73(b)**Applicant/Patent Owner: FEI CompanyApplication No./Patent No.: 6,185,707 B1 Filed/Issue Date: February 8, 2001Entitled: IC TEST SOFTWARE SYSTEM FOR MAPPING LOGICAL FUNCTIONAL TEST DATA OF LOGIC INTEGRATED CIRCUITS TO PHYSICAL REPRESENTATIONFEI Company, a Corporation  
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

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Reel 014805, Frame 0440, or for which a copy thereof is attached.
2. From: Shawn Smith To: Knights Technology, Inc.  
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The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Bradley J. Thies  
Signature  
Bradley J. Thies

7/19/05  
Date  
(503) 726-7500

Printed or Typed Name  
Vice President/General Counsel  
Title

Telephone Number

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**STATEMENT UNDER 37 CFR 3.73(b)**Applicant/Patent Owner: FEI CompanyApplication No./Patent No.: 6,185,707 B1 Filed/Issue Date: February 6, 2001Entitled: IC TEST SOFTWARE SYSTEM FOR MAPPING LOGICAL FUNCTIONAL TEST DATA OF LOGIC INTEGRATED CIRCUITS TO PHYSICAL REPRESENTATIONFEI Company, a Corporation  
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

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[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Bradley J. Thies

Signature

Bradley J. Thies

Printed or Typed Name

Vice President/General Counsel

Title

7/19/05

Date

(503) 726-7500

Telephone Number

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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US006185707B1

(12) **United States Patent**  
Smith et al.

(10) Patent No.: **US 6,185,707 B1**  
(45) Date of Patent: **Feb. 6, 2001**

(54) **IC TEST SOFTWARE SYSTEM FOR  
MAPPING LOGICAL FUNCTIONAL TEST  
DATA OF LOGIC INTEGRATED CIRCUITS  
TO PHYSICAL REPRESENTATION**

(75) Inventors: Shawn Smith, Austin; Hari  
Balachandran, Dallas; Jason Parker,  
Coppell, all of TX (US)

(73) Assignee: Knights Technology, Inc., Sunnyvale,  
CA (US)

(\*) Notice: Under 35 U.S.C. 154(b), the term of this  
patent shall be extended for 0 days.

(21) Appl. No.: 09/192,164

(22) Filed: Nov. 13, 1998

(51) Int. Cl.<sup>7</sup> ..... G01R 31/28

(52) U.S. Cl. .... 714/724; 382/145; 438/10;  
714/733

(58) Field of Search ..... 714/733, 737,  
714/26, 723, 724; 382/145, 149, 151, 168;  
250/559.4, 559.45; 356/237.4; 702/35, 84;  
700/79, 182; 324/614, 752, 500, 73.1, 754;  
438/10, 17, 975

(56) **References Cited**

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(List continued on next page.)

Primary Examiner—Albert De Cady

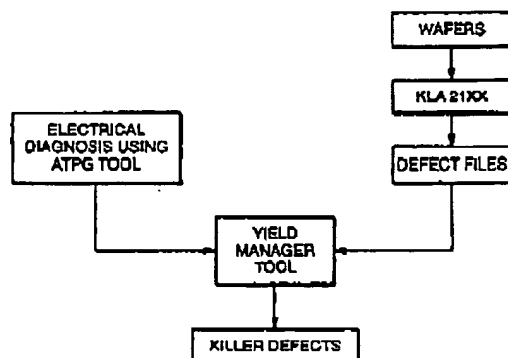
Assistant Examiner—Guy Lamarie

(74) Attorney, Agent, or Firm—Burns Doane Swecker & Mathis L.L.P.

#### (57) ABSTRACT

The present invention, generally speaking, takes advantage of the foregoing capability to determine and display the X,Y location corresponding to a net name, by translating functional test data of a digital logic chip passed through a simulation model which identifies one or more defective nets of the chip. The defective nets are processed against a database of the foregoing type to obtain X,Y coordinate data for these nets, allowing them to be data logged as physical traces on the chip layout. In accordance with an exemplary embodiment, this mapping is performed by taking the output from a functional tester and translating it from a list of failed scan chains into a list of suspected netlist nodes. The X,Y coordinates of suspected netlist nodes are then identified and stored in a database, providing failure analysis and yield enhancement engineers a starting point for performing failure analysis and for immediately understanding whether "in-line" inspection data can account for a given failure. These nodes may then be crossmapped from the circuit design onto the chip's layout for each of multiple photomask layers within the design. Detailed failure data is gathered and stored at the wafer stage as part of a comprehensive program rather than on an as-needed basis at the packaged part stage. A voluminous amount of high-quality data is therefore obtained in an entirely automated fashion, as opposed to obtaining a comparatively minuscule amount of lesser-quality data in an exceedingly laborious fashion.

9 Claims, 9 Drawing Sheets





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## PATENT APPLICATION INFORMATION RETRIEVAL



Search results as of: 7-1-2005:15:5:11 E.T.

Search results for patent number: 6,185,707			
Application Number:	09/192,164	Customer Number:	-
Filing or 371(c) Date:	11-13-1998	Status:	Patented Case
Application Type:	Utility	Status Date:	01-19-2001
Examiner Name:	LAMARRE, GUY J	Location:	FILE REPOSITORY (FRANCONIA)
Group Art Unit:	2784	Location Date:	03-23-2004
Confirmation Number:	9440	Earliest Publication No:	-
Attorney Docket Number:	014823-116	Earliest Publication Date:	-
Class/ Sub-Class:	714/724	Patent Number:	6,185,707
First Named Inventor:	SHAWN SMITH, AUSTIN, TX (US)	Issue Date of Patent:	02-06-2001
Title Of Invention:	IC TEST SOFTWARE SYSTEM FOR MAPPING LOGICAL FUNCTIONAL TEST DATA OF LOGIC INTEGRATED CIRCUITS TO PHYSICAL REPRESENTATION		

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File History	
Date	Contents Description
10-16-2000	Workflow - File Sent to Contractor
02-06-2001	Recordation of Patent Grant Mailed
01-19-2001	Issue Notification Mailed
01-07-2001	Application is Considered Ready for Issue
11-30-2000	Issue Fee Payment Verified
02-16-2000	Workflow - Drawings Finished
02-16-2000	Workflow - Drawings Matched with File at Contractor

1

02-16-2000	Workflow - Drawings Received at Contractor
01-02-2001	Workflow - Complete WF Records for Drawings
08-31-2000	Mail Notice of Allowance
08-31-2000	Notice of Allowance Data Verification Completed
08-28-2000	Notice of Allowability
06-22-2000	Examiner Interview Summary Record (PTOL - 413)
06-22-2000	Case Docketed to Examiner in GAU
06-22-2000	Date Forwarded to Examiner
06-08-2000	Response after Non-Final Action
06-08-2000	Request for Extension of Time - Granted
02-16-2000	New or Additional Drawing Filed
02-03-2000	Mail Non-Final Rejection
01-31-2000	Non-Final Rejection
03-22-1999	Case Docketed to Examiner in GAU
02-12-1999	Application Dispatched from OIPE
02-11-1999	Application Is Now Complete
12-07-1998	Notice Mailed—Application Incomplete—Filing Date Assigned
11-24-1998	IFW Scan & PACR Auto Security Review
11-18-1998	Initial Exam Team nn



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Patent #: 6185202

Issue Dt: 02/06/2001

Application #: 09192164

Filing Dt: 11/13/1998

Inventors: SHAWN SMITH, HARI BALACHANDRAN, JASON PARKER

Title: IC TEST SOFTWARE SYSTEM FOR MAPPING LOGICAL FUNCTIONAL TEST DATA OF LOGIC INTEGRATED CIRCUITS TO PHYSICAL REPRESENTATION

**Assignment: 1**

Reel/Frame: 014805/0440

Recorded: 07/01/2004

Pages: 3

Conveyance: MERGER (SEE DOCUMENT FOR DETAILS).

Assignor: KNIGHTS TECHNOLOGY, INC.

Exec Dt: 12/23/1998

Assignee: ELECTROGLASS, INC.

6024 SILVER VALLEY CREEK ROAD  
SAN JOSE, CALIFORNIA 95138

Correspondent: MICHAEL O. SCHEINBERG

P.O. BOX 164140

AUSTIN, TX 78746-4140

**Assignment: 2**

Reel/Frame: 009743/0549

Recorded: 02/05/1999

Pages: 3

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignor: SMITH, SHAWN

Exec Dt: 01/14/1999

Assignee: KNIGHTS TECHNOLOGY, INC.

155 NORTH WOLFE ROAD  
SUNNYVALE, CALIFORNIA 94086

Correspondent: BURNS, DOANE, SWECKER &amp; MATHIS, L.L.P.

MICHAEL J. URE

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ALEXANDRIA, VIRGINIA 22313-1404

**Assignment: 3**

Reel/Frame: 009733/0608

Recorded: 01/26/1999

Pages: 5

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Assignors: BALACHANDRAN, HARI

Exec Dt: 01/15/1999

PARKER, JASON

Exec Dt: 01/15/1999

Assignee: TEXAS INSTRUMENTS INCORPORATED

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Correspondent: TEXAS INSTRUMENTS INC.

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DALLAS, TX 75265

**Assignment: 4**

Reel/Frame: 014805/0456

Recorded: 07/01/2004

Pages: 6

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Exec Dt: 08/05/2003

Assignee: EEI COMPANY

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Correspondent: MICHAEL O. SCHEINBERG



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**Assignment: 5**

**Reel/Frame:** 014065/0082

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**Pages:** 5

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